HIGH-SPEED DIRECT SAMPLING FMC FOR BEAM DIAGNOSTIC AND ACCELERATOR PROTECTION APPLICATIONS

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AGENDA

1. DFMC-DS500 Digitizer Board
2. DAQ-System (Firmware / Software)
3. Coarse BAM Channel in FLASH
4. Test Measurements and Results
DFMC-DS500 Overview

- single width FMC according to ANSI/VITA 57.1 standard
- 8.5 mm stacking height
- air cooled, shielding cage + heatsink planned
- front panel: 5 RF SSMC + 1 HDMI Type D (micro) connectors
- 12-Bit, 500/800 MSP/s Dual Ch., 1/1.6 GSP/s Single Ch.
**DFMC-DS500 Overview**

- ADC input bandwidth: 2.7 GHz
- fully diff. amplifier [4,5] LS bandwidth: 4.8 GHz
- no anti-aliasing filter present
- variants with up to 3.2 GSP/s
• DFMC-DSX00-INTERFACE connected to LVDS data lanes → delay calibration
• DSX_PKT_GEN generates AXI stream packets readable by AXI DMA core

(see also THOA01, IBIC 2018, J.Marjanovic for data post-processing)

• AXI_DMA dumps data into DDR4 via AXI SmartConnect
• XDMA PCIe core controls cores via AXI Lite
• XDMA has full AXI connection to DDR4 via SMC → reads data from DDR4
- straight forward solution for DAQ
- XDMA transfers sample data from DDR4 (KCU105) into host PC’s RAM via PCIe root complex (DMA controller)
- Xilinx DMA driver (kernel space) provides pointer for DMA transfers into RAM
- Python library DSX00Lib can access transferred data in kernel space

- data can be dumped into file on SSD/HDD
- over 1 Mio. samples per channel can be stored on KCU105 (2GB DDR4)
- 8k samples can be stored on DAMC-FMC25 (256 MB DDR2)
Coarse BAM Channel

- Coarse BAM Channel planned in FLASH
- Coarse BAM channel in addition to electro-optical BAM [1,2] → automatically adjust optical delay lines
- Uses same combined high-bandwidth pick up [3] signals (40 GHz)
- Analog front end bandpass filters the pick up signal
- Bunch charges can vary from 20 pC up to 1 nC, which requires a dynamic range of about 34 dB
- Sampling (DFMC-DS500/DAMC-FMC25) and processing in MTCA.4 crate
CBAM Channel in FLASH

MOOB03, IBIC 2018, N. Baboi et al. for more details on FLASH

7th IBIC, Shanghai 2018
CBAM DS500 Test Setup

- complex high-bandwidth pick up signal
- testing ADC performance under ideal conditions with reduced signal bandwidth
- undersampling 1.3 GHz carrier with phase synchronous ADC clock → produces DC signal
- timing error converts into amplitude error
- roughly estimate the timing accuracy

Diagram:

- DRO 1.3 GHz
- Splitter
- Frequency Divider \(\div D \) (6)
- Phase Shifter
- 12-Slot MTCA Crate
- DAMC-FMC25
- DFMC-DS500
- ADC
- PLL × 2
- 433.33 MHz
- 2x DATA
- FPGA
- PCIe
- MCH
- PC
Results

- recorded 1.6M samples
- fitting normal distribution with:
  \[ \mu = -2.93117 \times 10^{-21} \text{s} \]
  \[ \sigma = 726.36 \text{ fs} \]
- timing error (p2p): 7 ps
- timing error (rms): 726 fs

- results are not outstanding but also not bad
- meet the requirements of ~1 ps
Summary & Outlook

• results of test measurements look promising
• meet the requirements of ~ 1 ps timing error
• operation in FLASH will show whether the accuracy will actually be achieved

• further improvements of the DFMC-DS500 have to be done → second revision
• PLL is not running with full performance (reduction of phase noise and jitter)
ACKNOWLEDGEMENTS


Thank you for your attention.
References


High-Speed Direct Sampling FMC for Beam Diagnostic and Accelerator Protection Applications

EOBAM System

BAM System's Units & Periphery

BAM: E0-Unit

BAM Box

Optical Clock

COL 0

COL 1

COL 2

TIM Coax

RF Generator

RF Amplifier

RF Attenuator

RF Filter

COMPARATOR

RF Output

DATA + TRIGGER

RF INPUT

BAM: Electronics-Unit

BAM: RF-Channel

RF Feedback

RF Tip

RF Mounting

RF Combining

RF Beam Pipe

Counter

BAM: RF-Unit

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